

SPECIFICATION AMENDMENTS:

Please replace the paragraph [0010] with the following replacement paragraph:

-- It is therefore an object of the invention to provide a method of forming a Type-I transistor and a Type-II transistor suitable for liquid crystal display (LCD). The method comprises the following procedures: providing a substrate; forming a first polysilicon layer and a second polysilicon layer corresponding to the Type-I transistor and the Type-II transistor respectively on the substrate; blanketly forming blanket depositing a gate insulating layer on the first polysilicon layer, the second polysilicon layer, and the substrate; forming a first gate and a second gate on the gate insulating layer respectively corresponding to the first polysilicon layer and the second polysilicon layer; performing a first doping using a first type dopant to form a first heavily doped region in the first polysilicon layer beside the first gate; and performing a second doping using a second type dopant to simultaneously form a second heavily doped region in the second polysilicon layer beside the second gate and form a lightly doped region in parts of the first heavily doped region beside the first gate, wherein the dosage of the second type dopant is smaller than that of the first type dopant.--

Please replace the paragraph [0011] with the following replacement paragraph:

-- Following the step of forming a lightly doped region of the Type-I transistor and a second heavily doped region of the Type-II transistor, the invention further comprises the following procedures: First, forming a 500 ~ 700 angstrom thick inner dielectric layer on the ~~gate oxide~~ gate insulating layer, the first gate and the second gate; second, selectively exposing the first heavily doped region, the second heavily doped region, the first gate and the second gate; third, forming an electrode includes either of Mo, Cr, and Ti/Al/Ti to be electrically connected to the exposed first heavily doped region, second heavily doped region, first gate and second gate.--

Please replace the paragraph [0021] with the following replacement paragraph:

-- Referring to FIG. 2B, a gate insulating layer, for example, a gate oxide 208, which can comprise SiO₂ with a thickness of 500 ~ 1500 angstroms, is blanketly-formed by blanket deposition on the buffer layer 202, the polysilicon layer 204(1), 204(2), and 204(3), and the substrate 200. Next, a conductive layer is deposited on the gate oxide 208, and gate 210(1), 210(2), 210(3), which can include Mo, Cr, or Ti/Al/Ti, are formed using photolithography and etching process. The gate 210(1), 210(2), 210(3) respectively correspond to the polysilicon layer 204(1), 204(2), and 204(3).--

Please replace the paragraph [0022] with the following replacement paragraph:

-- After that, in FIG. 2C, a patterned photoresist layer 212 is formed on substrate 200 through photolithography, wherein photoresist layer 212 covers up entire first PMOS transistor region which may form a CMOS transistor. Furthermore, photoresist layer 212 is used as a mask and a high concentration phosphorus dopant is implanted into substrate 200 to form heavily doped regions 204A, 204B, 204C, and 204D on the source/drain and lightly doped region of the first and second NMOS transistors, wherein the dosage of the phosphorus dopant is about 3e13 3e13 dosage/cm² ~ 5e15 5e15 dosage/cm². Meanwhile, the part of the source/drain region of the first and second NMOS transistors formed by heavily doped regions 204A, 204B, 204C, and 204D is exactly the source/drain of the first and second NMOS transistors. The heavily doped region 204A and 204B in the polysilicon layer 204(1) are formed beside the first gate 210(1), while the heavily doped region 204C and 204D in the polysilicon layer 204(3) are formed beside the first gate 210(3). This will be further elaborated after the procedures in FIG. 2D are completed.--

Please replace the paragraph [0023] with the following replacement paragraph:

--After that, in FIG. 2D, the remnants of photoresist layer 212 are removed and a patterned photoresist layer 214 is formed on gate oxide 208 through photolithography, wherein photoresist layer 214 covers up the source/drain region of the first NMOS transistor of the CMOS transistor as well as the source/drain region of the second NMOS transistor in pixel region, but not the first PMOS transistor region of the CMOS transistor. Furthermore, photoresist layer 214 is used as a mask and a high concentration boron dopant is implanted into substrate 200 to form heavily doped region 204i and 204j, the source/drain of the first PMOS transistor, as well as lightly doped regions 204m, 204n, 204x and 204y respectively in parts of the heavily doped region 204A, 204B, 204C, and 204D of the first and second NMOS transistors, wherein the dosage of boron dopant is about 3e13 3e13 dosage/cm² ~ 5e15 5e15 dosage/cm². The heavily doped regions 204i and 204j in the polysilicon layer 204(2) are formed beside the gate 210(2), the lightly doped regions 204m and 204n are formed beside the gate 210(1), and the lightly doped regions 204x and 204y are formed beside the gate 210(3). In heavily doped regions 204A, 204B, 204C, and 204D, the part other than lightly doped regions 204m, 204n, 204x, and 204y is exactly source/drain 204a, 204b, 204c and 204d of the NMOS transistor.--